UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,101	10/28/2003	Andras Szabo	010262-014410US	6613

20350 7590 10/30/2006

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
BUDD, PAUL A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,101	SZABO ET AL.	
	Examiner	Art Unit	
	Paul A. Budd	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *4 and 7-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims **1-3,** and **5-6** are pending in the instant application. Claims **4,** and **7-14** are cancelled. The objections to the specification are withdrawn and the amendments to the specification are accepted. The applicant did not address the 112(2nd) rejections of claims **1,5,** and **6** in the Office Action dated 20 March 2006. These rejections are repeated below and require appropriate action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim **1** recites the limitation "sufficiently long duration". There is no defined standard for this limitation and it is considered vague and indefinite. For the purposes of this office action the inherent delay defined by the claimed device structure is considered to be sufficient to meet the claimed device. It is the claimed structure that determines this delay.

Claims **5,6** recite the limitation "trimming circuit" in the beginning of the dependent claim. There is insufficient antecedent basis for this limitation in these claims or claim **1**. For the purposes of this office action the term "delay transistor" will be used in place of "trimming circuit".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1-3,** and **5-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Stein et al. (US Patent 4,725,747) in view of Matsuo el al. (US Patent 5,744,838).

Regarding claim **1**, Stein teaches a delay transistor [FIG. 1, 12] comprising:

a substrate [column 2, lines 6-7];

a plurality of conduction channels [FIG. 2, 50; the channel under the gates for sub-transistors 21a-21j, column 7, lines 2-3] embedded in the substrate;

a plurality of active regions [FIG. 1, 20a-20e (drains), 18a-18f (sources)] embedded in the substrate, the active regions alternating with the conduction channels [see FIG. 1];

a source contact [22, column 3, lines 22-23] coupled with first alternating active regions [20a-20e, 18a-18f];

a drain contact [22, column 3, lines 22-23] coupled with second alternating active regions; and

a gate structure [16] overlaying the conduction channels [as above], the gate structure [16] being configured to receive an external signal [see FIG. 1],

wherein the gate structure is a single [see FIG. 1, column 3, lines 16-21] gate structure, and

wherein the gate structure provides an RC delay [column 5, lines 6-14] to the external signal and filters power [column 2, lines 8-16] and voltage spikes [column 1 lines 57-64] in the external signal, the RC delay being of a sufficiently long duration so as to decrease the switching speed of the transistor and allow the gate structure to filter power and voltage spikes, wherein the delay transistor further comprises a plurality of *transistors* [FIG. 1, 40] coupled with the single gate structure [the serpentine gate 24], wherein the *transistors* [40] contribute additional capacitance [the *transistors'* source/drain junctions inherently add capacitance] to the RC delay.

However Stein does not teach "wherein the delay transistor further comprises a plurality of *diodes* coupled with the single gate structure, the *diodes* being reversed biased, wherein the *diodes* contribute additional capacitance to the RC delay. Matsuo does teach a plurality of diodes connected to a gate [FIG. 23, 106, 107,column 1-2, lines 58-3] in place of the plurality of transistors.

Stein and Matsuo are analogous art because they both are solving the problem of controlling voltage spikes adversely affecting circuits (Matsuo abstract "surge voltage", Stein abstract "voltage spikes"). It would have been obvious to one of ordinary skill in the art at the time that the invention was made to use a plurality of diodes in order to "prevent a gate oxide film of the initial input stage

logic circuit from deterioration or breaking by reducing the absolute value of the surge voltage" [column 1-2, lines 68-3].

Regarding the limitation "external signal" the broadest reasonable interpretation of "external signal" is interpreted as a signal external to the circuit structure claimed. The limitation "external signal" does not distinguish over the claimed structure.

Regarding claim **2**, Stein teaches the delay transistor of claim **1** wherein the gate structure has a serpentine shape [column 2, lines 29-32].

Regarding claim **3**, Stein teaches the delay transistor of claim **1** wherein the gate structure comprises polysilicon [column 3, lines 12-13 & lines 26-27].

Regarding claim **5**, Stein teaches the *delay transistor* of claim **1** wherein the delay transistor is an NMOS transistor [FIG. 1; 14; column 3, lines 26-27]. The gate structure is 24, the drain or source contacts are 30, and the plurality of active regions are the sources 26a-26d and drains 28a-28c.

Regarding claim **6**, Stein teaches the *delay transistor* of claim **1** wherein the delay transistor is a PMOS transistor [FIG. 1; 12; column 3, lines 12-13].

Response to Arguments

4. Applicant's arguments filed 14 August 2006 have been fully considered but they are not persuasive. With regards to the applicant's arguments of "input signal" versus "external signal", the broadest reasonable interpretation of "external signal" is interpreted as a signal external to the circuit structure claimed. The limitation "external signal" versus "input signal" does not distinguish over the claimed structure.

The applicant disputes the motivation for combining Matsuo and Stein. The motivation does not have to be the same as the applicant's motivation. The art is analogous art because they both are solving the problem of controlling voltage spikes adversely affecting circuits. The addition of diodes to the gates of MOSFETs is well known in the art for at least the purpose of preventing damage to MOSFET's gate oxide for ESD protection from plasma tools or from customer handling of MOSFETs.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number 571-272-8796. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N. DREW RICHARDS
PRIMARY EXAMINER